CLAIMS:

1. A semiconductor device comprising a substrate with a first and an opposed second side, at which first side a plurality of transistors and interconnects is present, which are covered by a protective security covering, which device is further provided with bond pad regions, characterized in that the protective security covering comprises a substantially non-transparent and substantially chemically inert security coating, and
the bond pad regions are accessible from the second side of the substrate.

2. A semiconductor device as claimed in Claim 1, characterized in that
- the bond pad regions are present on the first side of the substrate, and
- the substrate is a silicon substrate, that is patterned as required for access to the bond pad regions.

3. A semiconductor device as claimed in Claim 1 or 2, characterized in that a security layer is present at the second side of the substrate, which security layer leaves exposed the bond pad regions or any metallisation for access thereto.

4. A semiconductor device as claimed in Claim 1, characterized in that the bond pad regions protected against probing with antiprobe means.

5. A semiconductor device as claimed in Claim 1, characterized in that the security coating comprises a layer of TiO2.

6. A semiconductor device as claimed in Claim 1, characterized in that the security coating is formed of multiple alternate layers, which alternate layers are sensitive to different etchants.

7. A carrier comprising a semiconductor device according to Claim 1.

8. A method of manufacturing a semiconductor device provided with a substrate with a first and second side, comprising the steps of:

- providing a structure of transistors and interconnects at the first side of the substrate, the structure including bond pad regions that are defined at an interface with the substrate;
- applying a protective security covering including at least a substantially non-transparent and substantially chemically inert security coating;
- patterning the substrate from the second side so as to expose the bond pad regions.

9. A method according to Claim 8, wherein the substrate is a semiconductor substrate that is thinned and etched to expose the bond pad regions.

10. A method according to Claim 8 or 9, wherein a second substrate is provided on the protective security covering and attached to it by means of glue.